WHAT IS CLAIMED IS:

1. A delay time adjusting method of adjusting a delay time of an input signal so that a phase of said input signal and a phase of an output signal match each other, the method comprising the step of:

delaying said phase of said output signal until a phase difference between said phase of said input signal and said phase of said output signal becomes N periods, where N is an integer other than zero.

2. The delay time adjusting method as claimed in claim 1, further comprising a step of producing said output signal by delaying said input signal by a DLL circuit.

3. A delay time adjusting method of adjusting a delay time of an input first periodic signal so that a phase of said input first periodic signal and a phase of an output second periodic signal match each other, the method comprising the step of:

adjusting said delay time so that, when a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a predetermined rising edge of said input first

periodic signal, said predetermined rising edge of said output second periodic signal matches a rising edge of said input first periodic signal, a phase of the rising edge being behind and nearest to said phase of said predetermined rising edge of said output second periodic signal.

4. A delay time adjusting method of adjusting a delay time of an input first periodic signal so that a phase of said input first periodic signal and a phase of an output second periodic signal match each other, the method comprising:

a first step of judging whether a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a first rising edge of said input first periodic signal; and

a second step of delaying said phase of said output second periodic signal so that, when said phase of said predetermined rising edge is judged to be behind said phase of said first rising edge in said first step, said phase of said predetermined rising edge and a phase of a second rising edge of said input first periodic signal match each other, the second rising edge being one period behind said first rising edge.

5. A delay time adjusting circuit for adjusting a delay time of an input signal so that a phase of said input signal and a phase of an output signal match each other, the circuit comprising:

detecting means for detecting a phase

difference between said phase of said input signal and said phase of said output signal; and

delaying means for delaying said phase of said output signal until said phase difference becomes N periods, where N is an integer other than zero.

6. A delay time adjusting circuit for adjusting a delay time of an input first periodic signal so that a phase of said input first periodic signal and a phase of an output second periodic signal match each other, the circuit comprising:

judging means for judging whether a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a predetermined rising edge of said input first periodic signal; and

delaying means for adjusting said delay time so that, when said phase of said predetermined rising edge of said output second periodic signal is judged to be behind said phase of said predetermined rising edge of said input first periodic signal by said judging means, said predetermined rising edge of said output second periodic signal matches a rising edge of said input first periodic signal, a phase of the rising edge being behind and nearest to said phase of said predetermined rising edge of said output second periodic signal.

7. A delay time adjusting circuit for adjusting a delay time of an input first periodic signal so that a phase of said input first periodic

signal and a phase of an output second periodic signal match each other, the circuit comprising:

delaying means for delaying said input first periodic signal so as to generate said output second periodic signal;

phase-detecting means for detecting whether a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a first rising edge of said input first periodic signal; and

adjusting means for controlling said delaying means so that, when said phase of said predetermined rising edge is judged to be behind said phase of said first rising edge by said phase-detecting means, said delaying means delays said phase of said output second periodic signal until said phase of said predetermined rising edge and a phase of a second rising edge of said input first periodic signal match each other, the second rising edge being one period behind said first rising edge.

8. The delay time adjusting circuit as claimed in claim 7, wherein said adjusting means controls said delaying means so that, after said phase of said predetermined rising edge and said phase of said second rising edge match each other, said phase of said predetermined rising edge and said phase of said second rising edge match each other all the time within a tolerable range.